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10/709,467	05/07/2004	Che-Li Lin	12919-US-PA	3466

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
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EXAMINER	
PIZIALI, JEFFREY J	
ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/709,467	LIN, CHE-LI	
	Examiner	Art Unit	
	Jeff Piziali	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5,7-11,17 and 18* is/are pending in the application.

4a) Of the above claim(s) *5,9,10,17 and 18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,7,8 and 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 May 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. *Claims 1, 3, 7, 8, and 11* are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Kang et al (US 2002/0063666 A1)*** in view of the instant ***Application's Admitted Prior Art (AAPA)***.

Regarding claim 1, ***Kang*** discloses a color management structure [*Fig. 14*] for a panel display [*Fig. 14: 145*], comprising:

a display array unit [*Fig. 14: Clc*];

a plurality of gate drivers [*Fig. 14: 144*];

a plurality of source drivers [*Fig. 14: 143*],

said plurality of gate drivers and said plurality of source drivers driving said display array unit to display an image [*Fig. 14: video data*]; and

a timing sequence control unit [*Figs. 14 & 15: 142*],

said timing sequence control unit outputting a plurality of signals [*Figs. 14 & 15: Gsp, Dclk, RGB, γ data, clock*] to said plurality of gate drivers and said plurality of source drivers to drive said display array unit,

said timing sequence control unit outputting a clock signal [*Figs. 14 & 15: clock -- see also Fig. 9: I^2C clock, serial clock*] and

a digital color management data [*Figs. 14 & 15: γ data, aka User Selectable Gamma Modes A to D -- see also Fig. 9: I^2C Data*] to said plurality of source drivers (*see the entire document, including Paragraphs 69-74*),

said timing sequence control unit (*wherein Paragraph 70 states: "the timing/gamma controller 142 [in FIGs. 14 & 15] is integrated into a single chip incorporating the gamma controller 91 and the memory 92 in FIG. 9"*) comprising:

a timing controller [*Fig. 9: 91*] receiving a system input [*Fig. 9: from 100*] and providing said clock signal [*Fig. 9: I^2C Clock*]; and

a color management control block [*Fig. 9: 91*], coupled to said timing controller, outputting said digital color management data and said clock signal to said plurality of source drivers [*Fig. 8: 83; Fig. 9: 96-99; Fig. 14: 143; Fig. 15: 154-156*],

said digital color management data is adjustable [*Fig. 9: via 100*] (*e.g., wherein the Gamma Modes A to D are selectable/adjustable via the user interface*);

each of said plurality of source drivers comprising:

a source drive circuit [*Fig. 9: 97; Fig. 15: 156*] to drive said display array unit; and

a programmable data interface [*Fig. 9: 92, 93; Fig. 15: memory within 142, 152*] receiving said digital color management data [*Fig. 9: I^2C Data; Fig. 15: γ data*] and said clock signal [*Fig. 9: I^2C Clock; Fig. 15: Clock*] to parallel output a plurality of color voltage level signals [*Figs. 9, 10: GMA*] to said source drive circuit (*see the entire document, including Paragraphs 48-61*).

Should it be shown that ***Kang*** discloses the claimed subject matter of "*gate/source drivers*" with insufficient specificity:

The ***AAPA*** discloses a color management structure [*Fig. 2*] for a panel display [*Fig. 2: 120*], comprising:

a display array unit [*Fig. 2: pixel array*];

a plurality of gate drivers [*Fig. 2: 124*];

a plurality of source drivers [*Fig. 2: 122*],

said plurality of gate drivers and said plurality of source drivers driving said display array unit to display an image; and

a timing sequence control unit [*Fig. 2: 126*],

said timing sequence control unit outputting a plurality of signals [*Fig. 2: clock & color data from 126 to 122 & 124*] to said plurality of gate drivers and said plurality of source drivers to drive said display array unit,

said timing sequence control unit outputting a clock signal [*Fig. 2: clock*] and

a digital color management data [*Fig. 2: color data*] to said plurality of source drivers (*see the entire **AAPA**, including Paragraphs 7-10*).

Kang and the ***AAPA*** are analogous art, because they are from the shared inventive field of driving, timing control, and gamma correction of liquid crystal displays.

Therefore, it would have been obvious to use the ***AAPA's*** gate/source drivers in the place of ***Kang's*** gate/source drivers, because the substitution of one known arrangement of gate/source drivers for another would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

See KSR International Co. v. Teleflex Inc., et al., Docket No. 04-1350 (U.S. 30 April 2007).

Regarding claim 3, ***Kang*** discloses said panel display is a liquid crystal display (*see the entire document, including Paragraph 69*).

Regarding claim 7, ***Kang*** discloses said plurality of color voltage level signals includes a plurality of color gamma voltage level data (*see the entire document, including Paragraphs 48-61 -- for red, green, and blue video data*).

Regarding claim 8, ***Kang*** discloses said programmable data interface includes:

an input interface [*Fig. 9: 92*] receiving said digital color management data [*Fig. 9: I^2C Data*] and said clock signal [*Fig. 9: I^2C Clock*] and translating said digital color management data [*Fig. 9: 6-bit serial gamma data*] via a data format;

a decoder [*Fig. 10: 101*] receiving said translated digital color management data and said clock signal and decoding said translated digital color management data, and outputting a decoded data [*Fig. 11: D5-D0*] and a control signal [*Fig. 11: A3-A0, SD-SA*]; and

a digital-to-analog converting unit [*Fig. 10: 103*] receiving said decoded data, said control signal, and said clock signal, and parallel outputting said plurality of color voltage level signals (*see the entire document, including Paragraphs 48-61 -- for red, green, and blue video data*).

The ***AAPA*** additionally discloses a digital-to-analog converting unit [*Fig. 1: 106*] receiving decoded data [*Fig. 1: VGMA1-VGMA14*], a control signal [*Fig. 1: POL*], and a clock signal [*Fig. 1: CLK1*], and parallel outputting a plurality of color voltage level signals [*Fig. 1: Y1-Y384*] (*see the entire **AAPA**, including Paragraphs 7-10*).

Regarding claim 11, ***Kang*** discloses said timing sequence control unit is integrated into an application specified integrated circuit (*see the entire document, including Paragraph 70*).

The ***AAPA*** additionally discloses said timing sequence control unit is integrated into an application specified integrated circuit [*Fig. 2: ASIC*] (*see the entire **AAPA**, including Paragraphs 7-10*).

4. *Claims 3 and 11* are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Kang et al (US 2002/0063666 A1)*** and the instant ***Application's Admitted Prior Art (AAPA)*** as applied to *claim 1* above, and further in view of ***Lee (US 6,429,841 B1)***.

Regarding claim 3, ***Kang*** discloses said panel display is a liquid crystal display (*see the entire document, including Paragraph 69*).

Should it be shown that the combination of the ***AAPA*** and ***Kang*** teaches a liquid crystal display and each of the source drivers comprising a source drive circuit and a programmable data interface with insufficient specificity:

Lee discloses a color management structure [*e.g., Fig. 7*] for a liquid crystal display [*e.g., Fig. 7: 10*], comprising:

a plurality of source drivers [*e.g., Fig. 7: DIC1 + 16A, DIC2 + 16C, DICj + 16B*],

each of said plurality of source drivers comprising:

a source drive circuit [*e.g., Fig. 7: DIC1, DIC2, or DICj*] to drive said display array unit; and

a gamma voltage generator [*e.g., Fig. 7: 16A, 16C, or 16B*] to parallel output a plurality of color voltage level signals [*Fig. 13: OL1-OLk*] to said source drive circuit (*see the entire document, including Column 7, Line 13 - Column 9, Line 10; Column 13, Lines 30-55*).

Kang, the ***AAPA***, and ***Lee*** and are analogous art, because they are from the shared inventive field of driving, timing control, and gamma correction of liquid crystal displays.

Therefore, it would have been obvious to use ***Lee's*** technique of combining plural gamma voltage generators [*e.g., Fig. 7: 16A, 16C, or 16B*] with plural source driver circuits [*e.g., Fig. 7: DIC1, DIC2, or DICj*] to form ***Kang's*** color management structure as a combination of plural gamma voltage generators [*e.g., Figs. 8, 9: 84; Fig. 15: 142, 152, 153*] and plural source driver circuits [*e.g., Figs. 8: 83; Fig. 14: 143*], so as to compensate the applied difference in the applied signal to substantially eliminate the flickering and residual image effects [*e.g., see* ***Lee:*** *Column 3, Line 65 - Column 4, Line 50*].

Regarding claim 11, ***Kang*** discloses said timing sequence control unit is integrated into an application specified integrated circuit (*see the entire document, including Paragraph 70*).

The ***AAPA*** additionally discloses said timing sequence control unit is integrated into an application specified integrated circuit [*Fig. 2: ASIC*] (*see the entire* ***AAPA****, including Paragraphs 7-10*).

Should it be shown that the combination of the ***AAPA*** and ***Kang*** teaches an application specified integrated circuit and each of the source drivers comprising a source drive circuit and a programmable data interface with insufficient specificity:

Lee discloses a color management structure [*e.g., Fig. 7*] for a liquid crystal display [*e.g., Fig. 7: 10*], comprising:

a plurality of source drivers [*e.g., Fig. 7: DIC1 + 16A, DIC2 + 16C, DICj + 16B*],

each of said plurality of source drivers comprising:

a source drive circuit [*e.g., Fig. 7: DIC1, DIC2, or DICj -- which are integrated circuits*] to drive said display array unit; and

a gamma voltage generator [*e.g., Fig. 7: 16A, 16C, or 16B*] to parallel output a plurality of color voltage level signals [*Fig. 13: OL1-OLk*] to said source drive circuit (*see the entire document, including Column 7, Line 13 - Column 9, Line 10; Column 13, Lines 30-55*).

Kang, the ***AAPA***, and ***Lee*** and are analogous art, because they are from the shared inventive field of driving, timing control, and gamma correction of liquid crystal displays.

Therefore, it would have been obvious to use ***Lee's*** technique of combining plural gamma voltage generators [*e.g., Fig. 7: 16A, 16C, or 16B*] with plural source driver circuits [*e.g., Fig. 7: DIC1, DIC2, or DICj*] to form ***Kang's*** color management structure as a combination of plural gamma voltage generators [*e.g., Figs. 8, 9: 84; Fig. 15: 142, 152, 153*] and plural source driver circuits [*e.g., Figs. 8: 83; Fig. 14: 143*], so as to compensate the applied difference in the applied signal to substantially eliminate the flickering and residual image effects [*e.g., see **Lee:** Column 3, Line 65 - Column 4, Line 50*].

Response to Arguments

5. Applicant's arguments filed on *15 December 2009* have been fully considered but they are not persuasive.

The Applicant contends, "*the programmable data interface 92, 93 in Fig. 9 of **Kang** is disposed outside the source driver 97. That is, **Kang** discloses only one set of the programmable*

data interface 92, 93 for providing GAMMA voltages to all of the source drivers" (see Page 8, Paragraph 1 of the Response filed on *15 December 2009*). However, the examiner respectfully disagrees.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (*i.e., disposing the programmable data interface inside the source driver and/or plural sets of programmable data interfaces for providing GAMMA voltages to all of the source drivers*) are not recited in the rejected claims.

The Applicant contends, "*all the source drivers are programmed through the programmable data interface thereof, and the GAMMA voltages (color voltage level signals) used by all of the source drivers are different*" (see Page 8, Paragraph 2 of the Response filed on *15 December 2009*). However, the examiner respectfully disagrees.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (*i.e., the GAMMA voltages (color voltage level signals) used by all of the source drivers are different*) are not recited in the rejected claims.

The Applicant contends, "*the programming interfaces are embedded in each of the source drivers separately in the amended claim 1*" (see Page 9, Paragraph 1 of the Response filed on *15 December 2009*). However, the examiner respectfully disagrees.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (*i.e., the programming interfaces are embedded in each of the source drivers separately in the amended claim 1*) are not recited in the rejected claims.

Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Kang discloses a plurality of source drivers [*Fig. 14: wherein the column driver 143 includes distinct address shift register, latch, DAC, and buffer circuitry (see Fig. 2) for each data line column DL1-DLn of the display panel 145*],

each of said plurality of source drivers comprising:

a source drive circuit [*Fig. 9: voltage follower 97; Fig. 15: voltage follower 156 -- providing a single buffered data voltage signal to a single data line column DL -- see paragraph 12, line 6*] to drive said display array unit; and

a programmable data interface [*Fig. 9: memory 92, multi-channel DAC 93; Fig. 15: memory included within timing/gamma controller 142, multi-channel DAC 152*] receiving digital color management data [*Fig. 9: I^2C Data; Fig. 15: γ data*] and clock signal [*Fig. 9: I^2C Clock; Fig. 15: Clock*] to parallel output a plurality of color voltage level signals [*Figs. 9, 10: gamma reference voltages GMA*] to said source drive circuit

(*see the entire document, including Paragraphs 48-61*).

Firstly, each of ***Kang's*** Figures 9 and 15 illustrate a circuit having a single voltage follower [*Fig. 9: 97; Fig. 15:156*] outputting a single display data voltage to a single data line [*DL1*].

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention that a second data line [*DL2*] of ***Kang's*** LCD panel [*Fig. 8: 86; Fig. 14:145*] would require a second duplicate circuit (*as illustrated in Figures 9 and 15*) attached to it.

Accordingly, each of the other data lines [*DL3-DLn*] of ***Kang's*** LCD panel [*Fig. 8: 86; Fig. 14:145*] would have their own respective circuit (*as illustrated in Figures 9 and 15*) attached to them.

Secondly, even if arguably, all of ***Kang's*** data lines were shown to share a single programmable data interface; such an arrangement still reads on the instant claims.

For example, the instant claims do not specify that each of said plurality of source drivers comprises a source drive circuit separate and distinct from the source drive circuits of the other source drivers.

Similarly, the instant claims do not specify that each of said plurality of source drivers comprises a programmable data interface separate and distinct from the programmable data interfaces of the other source drivers.

At present there is no claim language preventing each of said plurality of source drivers from comprising a common source drive circuit and a common programmable data interface, shared by all the other source drivers.

Thirdly, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In the event that it were arguably shown that ***Kang*** discloses the claimed subject matter of "*plural source drivers*" with insufficient specificity, the instant ***Application's Admitted Prior Art (AAPA)*** has been relied upon.

The ***AAPA*** discloses a plurality of separate and distinct LCD source drivers [*Fig. 2: 122*].

In this scenario, ***Kang*** is seen as disclosing a single LCD source driver, comprising: a single column driver [*Fig. 8: 83; Fig. 14: 143*] combined with a single multi-mode gamma voltage generator [*Fig. 8: 84; Fig. 14: 142*].

Therefore, applying the ***AAPA's*** teaching of multiple source drivers to ***Kang*** would obviously result in plural "*column driver + gamma voltage generator*" [*Fig. 8: 83+84; Fig. 14: 142+143*] combinations.

Fourthly, a structure simply comprising multiple/extra copies of ***Kang's*** disclosed circuits would be deemed obvious to one having ordinary skill in the art at the time of invention.

It would have been obvious to one of ordinary skill in the art at the time of invention, because a person of ordinary skill has good reason to pursue the known options within his or her

technical grasp (*i.e., making duplicate copies of known circuits*). If this leads to the anticipated success, it is likely the product is not of innovation but of ordinary skill and common sense.

Fifthly, ***Kang's*** circuitry could be further divided to read on the instantly claimed subject matter. For example:

Kang discloses a plurality/pair of source drivers [*Fig. 14: wherein the column driver 143 includes distinct address shift register, latch, DAC, and buffer circuitry (see Fig. 2) for a first data line column DL1 and for a second data line column DL2*],

the first of said plurality/pair of source drivers comprising:

a first source drive circuit [*Fig. 9: voltage follower 97 -- providing a first buffered data voltage signal to a first data line column DL1*] to drive said display array unit; and

a first programmable data interface [*Figs. 9, 10: a first multi-mode gamma data set within memory 92 provided to multi-channel DAC 93 for analog conversion*] receiving the digital color management data [*Fig. 9: I^2C Data; Fig. 15: γ data*] and the clock signal [*Fig. 9: I^2C Clock; Fig. 15: Clock*] to parallel output a plurality of color voltage level signals [*Figs. 9, 10: gamma reference voltages GMA1-GMA4*] to said first source drive circuit; and

the second of said plurality/pair of source drivers comprising:

a second source drive circuit [*Fig. 9: voltage follower 97 -- providing a second buffered data voltage signal to a second data line column DL2*] to drive said display array unit; and

a second programmable data interface [*Figs. 9, 10: a second multi-mode gamma data set within memory 92 provided to multi-channel DAC 93 for analog conversion*] receiving the digital color management data [*Fig. 9: I^2C Data; Fig. 15: γ data*] and the clock signal [*Fig. 9:*

I^2C Clock; Fig. 15: Clock] to parallel output a plurality of color voltage level signals [*Figs. 9, 10: gamma reference voltages GMA5-GMA8*] to said second source drive circuit.

Sixthly, the Applicant's attention is respectfully pointed to the teachings of ***Lee (US 6,429,841 B1)***.

Lee discloses a color management structure [*e.g., Fig. 7*] for a liquid crystal display [*e.g., Fig. 7: 10*], comprising:

a plurality of source drivers [*e.g., Fig. 7: DIC1 + 16A, DIC2 + 16C, DICj + 16B*],

each of said plurality of source drivers comprising:

a source drive circuit [*e.g., Fig. 7: DIC1, DIC2, or DICj*] to drive said display array unit; and

a gamma voltage generator [*e.g., Fig. 7: 16A, 16C, or 16B*] to parallel output a plurality of color voltage level signals [*Fig. 13: OL1-OLk*] to said source drive circuit (*see the entire document, including Column 7, Line 13 - Column 9, Line 10; Column 13, Lines 30-55*).

Therefore, it was well known and commonly understood at the time of invention in the field of liquid crystal displays to:

provide a first source driver [*e.g., Fig. 7: DIC1*] with a first gamma voltage generator [*e.g., Fig. 7: 16A*];

provide a second source driver [*e.g., Fig. 7: DIC2*] with a second gamma voltage generator [*e.g., Fig. 7: 16C*]; and

provide a third source driver [*e.g., Fig. 7: DICj*] with a third gamma voltage generator [*e.g., Fig. 7: 16B*].

Kang, the ***AAPA***, and ***Lee*** and are analogous art, because they are from the shared inventive field of driving, timing control, and gamma correction of liquid crystal displays.

Therefore, it would have been obvious to use ***Lee's*** technique of combining plural gamma voltage generators [*e.g., Fig. 7: 16A, 16C, or 16B*] with plural source driver circuits [*e.g., Fig. 7: DIC1, DIC2, or DICj*] to form ***Kang's*** color management structure as a combination of plural gamma voltage generators [*e.g., Figs. 8, 9: 84; Fig. 15: 142, 152, 153*] and plural source driver circuits [*e.g., Figs. 8: 83; Fig. 14: 143*], so as to compensate the applied difference in the applied signal to substantially eliminate the flickering and residual image effects [*e.g., see* ***Lee:*** *the Abstract and Column 3, Line 65 - Column 4, Line 50*].

In response to applicant's argument that "*the panel display disclosed by newly amended claim 1 overcomes the problem of the variations of each of the columns caused by the process of programming different color voltage level signals to each of the source drive circuits*" (see Page 8, Paragraph 3 of the Response filed on *15 December 2009*), the arguable fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (*i.e., programming*

different color voltage level signals *to each of the source drive circuits*) are not recited in the rejected claims.

Applicant's arguments with respect to *claims 1, 3, 7, 8, and 11* have been considered but are moot in view of the new ground(s) of rejection.

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeff Piziali/
Primary Examiner, Art Unit 2629
22 March 2010